Using TVS to Verify SpaceWire Designs

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Agenda

- Introduction
- Commercial off-the-shelf (COTS) SpaceWire (SpW)Test Equipment (TE)
- Total Verification System (TVS) SpW TE
  - TVS Field Programmable Gate Array (FPGA)
  - TVS Usage
- TVS Usage Results
- TVS Commercialization
- TVS Availability

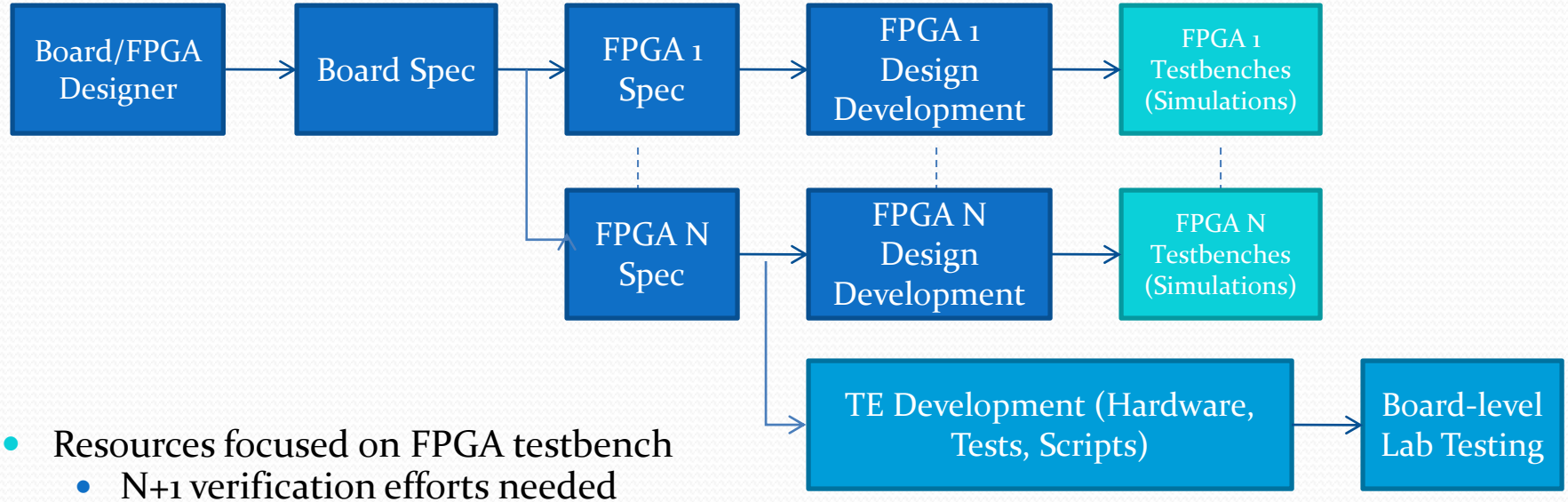
Introduction

- Is it necessary to improve upon the SpW verification process already in place?
- What's wrong with using COTS equipment?
- Is it possible to have a faster, cheaper, **and** better way of verifying SpW Designs?

COTS SpW TE

- What's missing?
  - Simulation models
    - Board designs are becoming more Field Programmable Gate Array (FPGA)-centric
    - Board level simulations require driving SpW interfaces with *something*
  - Ease of Customization
    - Designs usually contain mixed I/O
      - SpW
      - Low Voltage Transistor Transistor Logic (LVTTL)
      - TTL
      - RS422
    - Requirement Flexibility
      - SpW Timecodes
      - Built in Bit Error Rate Feature

Common Verification Process



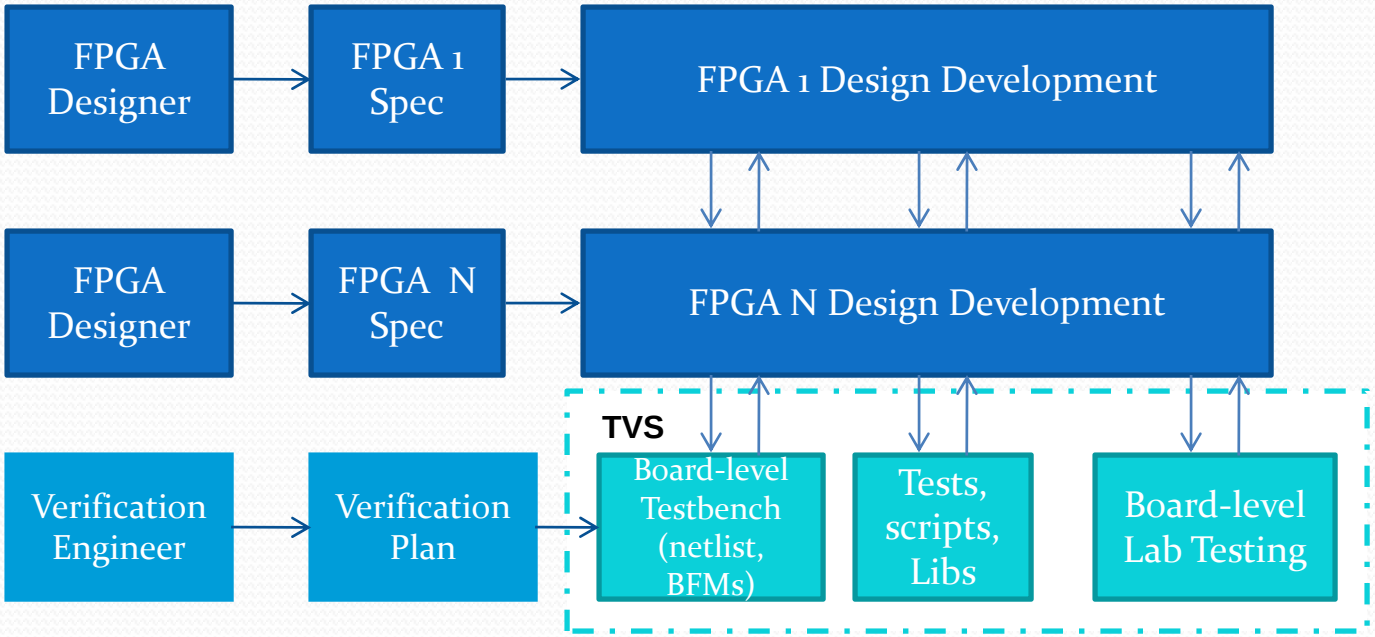
- Resources focused on FPGA testbench
  - N+1 verification efforts needed
- Serialized effort for FPGA design and verification
  - Takes more time with lower fidelity results
  - Mitigating time requires more manpower
- Redundant testbench elements developed
  - Between FPGA testbenches and board-level TE/testing
- Bugs found at board level must be recreated in FPGA testbench
  - May require development of new FPGA testbench capability to expose corner case bug
- No good metric for measuring thoroughness of board testing
- Code coverage results from simulation do not apply to lab tests

Motivation For A New Approach

- Move to Board Level Simulations
  - Reduce number of testbenches from N+1 to 1
  - All FPGAs simulated together
  - FPGA-level simulation only on reusable IP cores (RMAP, SpaceWire, etc)
  - Create simulation models for all relevant non-programmable devices
  - Bus Functional Models (BFM) represent TE

- Portability From Simulation to Lab
  - Mitigate redundantly developed resources
  - Create accurate TE simulation models
    - Use customizable TE
  - Use synthesizable VHDL BFMs
- Simulation-intensive
  - Ensure that majority of bugs are found in simulation
  - Suite of tests to obtain 100% Register Transfer Level (RTL) statement coverage on non-reusable IP
  - Reduces costly time spent debugging in the lab

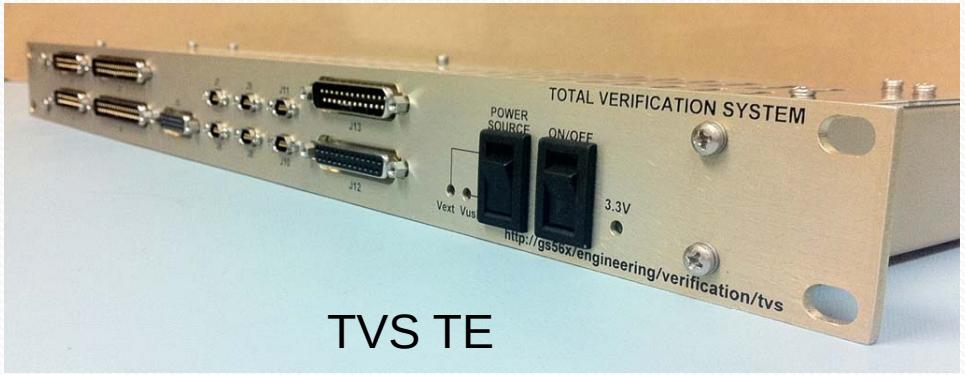
New Verification Process



- Reduced Verification Effort (1 vs. N+1)
- Parallel Design Flow Process
- Incremental Design Verification Review
- High Fidelity Process
  - Promotes code reuse (Same testbench used in simulation and lab testing)
- Collaborative Effort
  - Design not simply thrown over the fence.
  - Verification Engineer and FPGA Designer work together to verify the design.
- Code Coverage Results Apply to Lab Tests as well

TVS

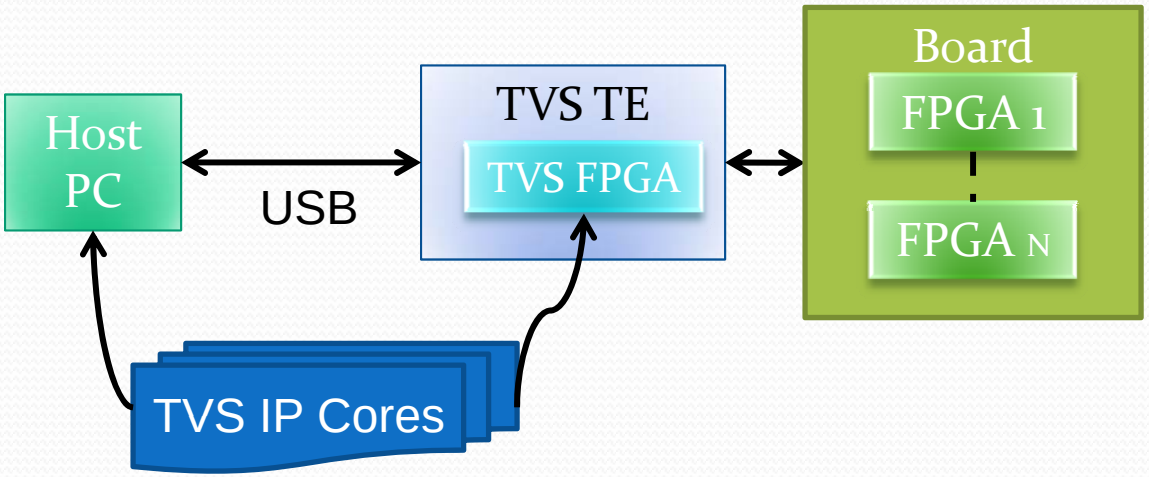
- Total
  - For use throughout design phases
- Verification
  - Used to verify designs
- System
  - Not just a piece of test equipment for the lab
  - Development starts in simulation and is used at board-level testing
  - Includes software applications ranging from directed tests to Labview-like GUI programs



TVS TE

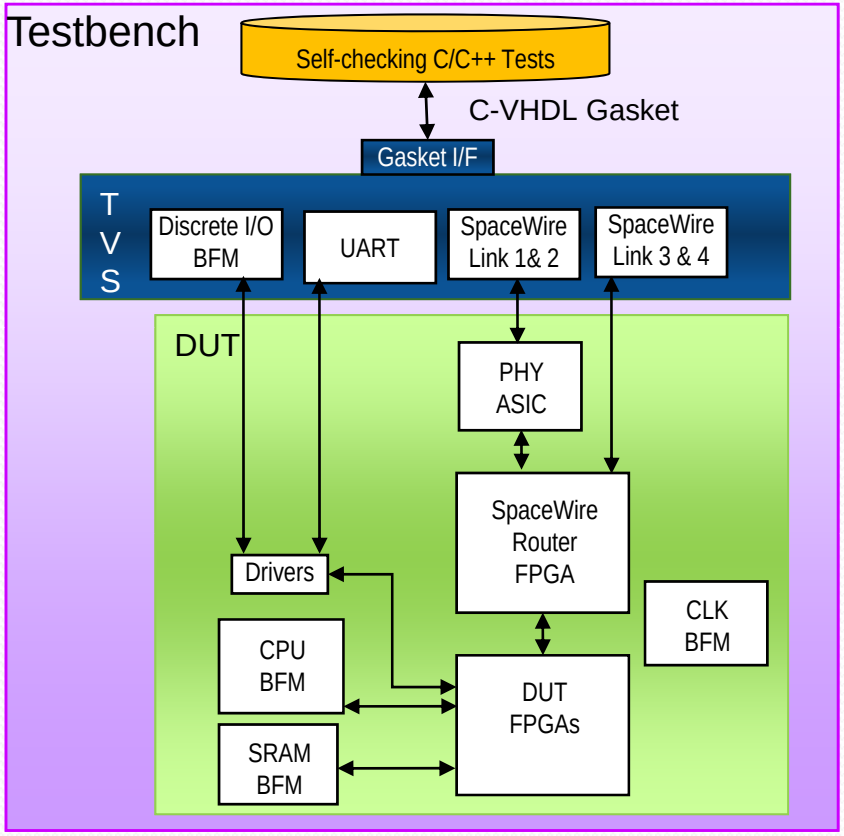
TVS Overview

- The TVS contains a USB-programmable Xilinx Spartan 3 FPGA that implements part of the board-level test bench
- The TVS contains many common IO signals (LVDS, RS422, TTL, LVTTL)
  - LVDS – 12 out, 12 in (on 6 MDM-9 connectors)
  - RS422 – 20 out, 44 in (on 5 D-sub connectors)
  - TTL/LVTTL Outputs – 20 (3.3V/5V selectable in groups of 4)
  - Digital Inputs – 8 (accepts 3.3V – 15V)
- A host PC runs directed tests that drive the TVS over USB
  - Self-checking, automated tests
- Libraries of TVS IP cores (VHDL and C++) available for quick testbench generation



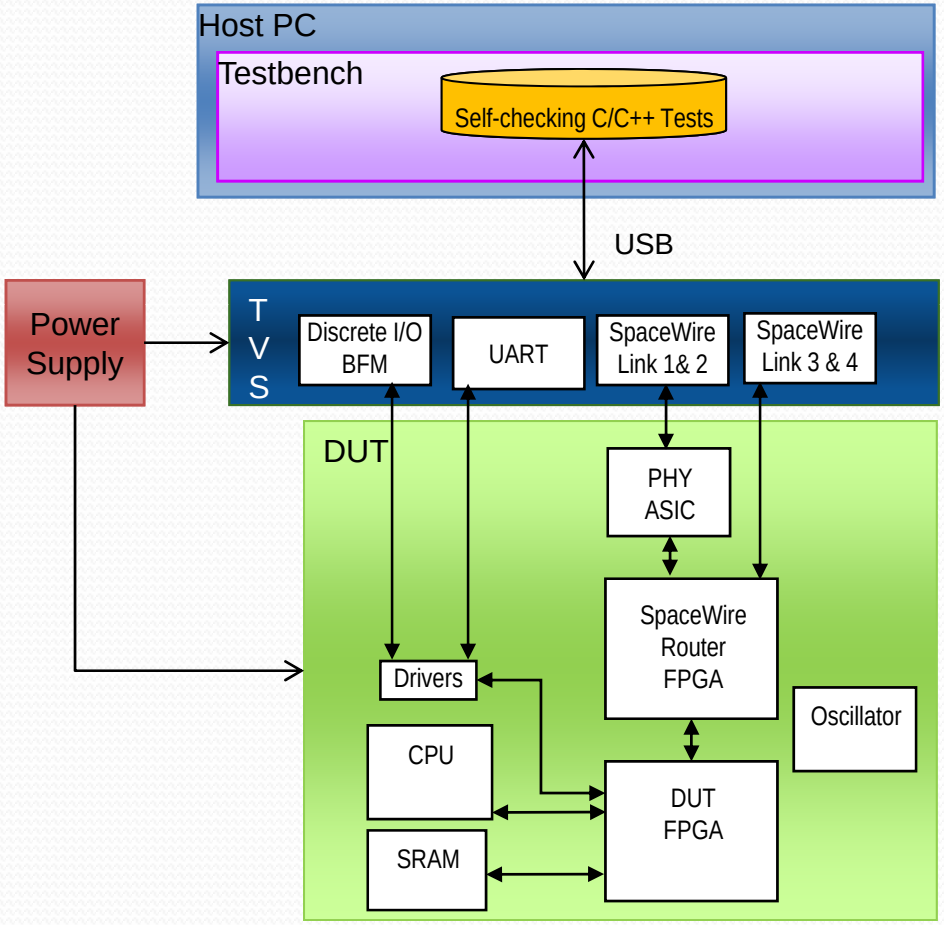
TVS in Simulation Environment

- Tests are used for simulation and lab testing
  - Tests only communicate with TE
- C-VHDL Gasket bridges tests to simulator
  - Gasket Interface used for every TE model
- TVS BFMs
  - Standard Blocks (SpW, UART)
  - Mission-specific Blocks
- Device Under Test (DUT) contains FPGA RTL code and device models



TVS In Lab Environment

- Tests taken from simulation
  - Tests only communicate to TE
- TE Models replaced with actual TE
- TVS BFMs are targeted to TVS FPGA
- DUT
  - Breadboard for development
  - Flight for testing



TVS Usage Results

- TE Cost Savings
  - TVS replaced Front End Data System (FEDS)
  - TVS replaced SpaceWire Test Set (SWTS)
- Bugs Found
  - In Simulation (average)
    - Board Level – 41
  - In Lab (average)
    - Board Level – 3
    - Box Level – 3
- Lab Time
  - Typically, 80-90% of board functionality tested in 1-2 weeks after delivery of board and safe-to-mate testing
    - Lunar Reconnaissance Orbiter Mission
    - Global Precipitation Measurement Mission
    - Magnetospheric MultiScale Mission
- Lessens Possibilities of Board Respin

TVS Commercialization

- Potential Product Markets
  - Space
  - Military
  - Medical
  - Automotive
- Training Classes
  - Tutorials
  - Webinars
  - Seminars
  - On-site Training
  - One on One Consultation
- Usage for Design Verification Services
  - Competitive Advantage
  - Increase Design Quality and Reliability

TVS Availability

- Hardware
  - NASA can license out the design files necessary for fabrication
  - Estimated costs
    - Parts and Fabrication~$1k
    - Retail Price ~ $5k would be acceptable
- Software
  - Test bench software comes with the hardware
  - FPGA IP cores (VHDL and DLLs) can be licensed for use
    - License can run anywhere from $500 - $5k per use

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